What is claimed is:

1. A semiconductor memory device, comprising:

a lower electrode;

a composite dielectric layer including an Al_2O_3 dielectric layer and an HfO_2 dielectric layer sequentially formed on the lower electrode, the Al_2O_3 dielectric layer having a thickness greater than or equal to the HfO_2 dielectric layer; and

an upper electrode formed on the composite dielectric layer.

2. The semiconductor device of claim 1, wherein the Al_2O_3 dielectric layer has a thickness of 30-60Å.

3. The semiconductor device of claim 1, wherein the HfO_2 dielectric layer has a thickness of 40Å or less.

4. The semiconductor device of claim 3, wherein the HfO_2 dielectric layer has a thickness of 10-40Å.

5. The semiconductor device of claim 1, wherein the lower electrode is made of one of polysilicon, metal nitride, and noble metal.

6. The capacity of claim 5, wherein the lower electrode is made of one selected from the group consisting of TiN, TaN, WN, Ru, Ir, Pt, and a composite layer of the forgoing materials.

7. The semiconductor device of claim 1, wherein the upper electrode is made of one of polysilicon, metal nitride, and noble metal.

8. The semiconductor device of claim 7, wherein the upper electrode is made of one selected from the group consisting of TiN, TaN, WN, Ru, Ir, Pt, and a composite layer of the forgoing materials.

9. The semiconductor device of claim 1, wherein the lower electrode is made of polysilicon, and a silicon nitride layer is further formed between the lower electrode and the composite dielectric layer.

10. A semiconductor memory device, comprising:

a lower electrode made of one of metal nitride and noble metal;

an upper electrode made of one of metal nitride and noble metal;

a composite dielectric layer, formed between the lower electrode and the upper electrode, that includes an Al_2O_3 dielectric layer and an HfO_2 dielectric layer with a thickness ratio of Al_2O_3 to HfO_2 that is greater than or equal to 1.

11. The semiconductor device of claim 10, wherein the Al_2O_3 dielectric layer has a thickness of 30-60Å.

12. The semiconductor device of claim 10, wherein the HfO_2 dielectric layer has a thickness of 40Å or less.

13. The semiconductor device of claim 12, wherein the HfO_2 dielectric layer has a thickness of 10-40Å.

14. The semiconductor device of claim 10, wherein the lower electrode is made of one selected from the group consisting of TiN, TaN, WN, Ru, Ir, Pt, and a composite layer of the forgoing materials.

15. The semiconductor device of claim 10, wherein the upper electrode is made of one selected from the group consisting of TiN, TaN, WN, Ru, Ir, Pt, and a composite layer of the forgoing materials.

16. A method of manufacturing a semiconductor memory device, the method comprising:

forming a lower electrode on a semiconductor substrate;

forming a composite dielectric layer on the lower electrode, the composite dielectric layer including an Al_2O_3 dielectric layer having a first thickness and an HfO_2 dielectric layer having a second thickness, the second thickness being smaller than or equal to the first thickness; and

forming an upper electrode on the composite dielectric layer.

17. The method of claim 16, wherein the Al_2O_3 dielectric layer is formed using one of chemical vapor deposition and atomic layer deposition.

18. The method of claim 16, wherein the first thickness of the Al_2O_3 dielectric layer is in a range of 30-60Å.

19. The method of claim 16, wherein the HfO_2 dielectric layer is formed using one of chemical vapor deposition and atomic layer deposition.

20. The method of claim 16, wherein the second thickness of the HfO_2 dielectric layer is smaller than or equal to 40Å.

21. The method of claim 20, wherein the second thickness of the HfO_2 dielectric layer is in a range of 10-40Å.

22. The method of claim 16, wherein the lower electrode is made of one of polysilicon, metal nitride, and noble metal.

23. The method of claim 22, wherein the lower electrode is made of one selected from the group consisting of TiN, TaN, WN, Ru, Ir, Pt, and a composite layer of the forgoing materials.

24. The method of claim 16, wherein the upper electrode is made of one of polysilicon, metal nitride, and noble metal.

25. The method of claim 24, wherein the upper electrode is made of one selected from the group consisting of TiN, TaN, WN, Ru, Ir, Pt, and a composite layer of the forgoing materials.

26. The method of claim 16, further comprising thermally treating the composite dielectric layer.

27. The method of claim 26, wherein thermally treating the composite dielectric layer is performed in a vacuum, in an oxygen atmosphere, in an inert gas atmosphere by rapid thermal annealing, by furnace annealing, plasma annealing, or UV annealing.